

Table Of Contents	
01	CHANGELIST & TOC
02	BLOCK DIAGRAM
03	POWER
04	SD CARD INTERFACE (UHS-II)
05	USB 3.0 HUB INTERFACE
06	SLIO B2B INTERFACE
07	DEBUG & TEST POINTS
08	MECHANICAL NOTES
09	
10	
11	
12	
13	
14	
15	
16	
17	

CAD Note:

Property: BUILD-OPT

ALL = Installed Part.

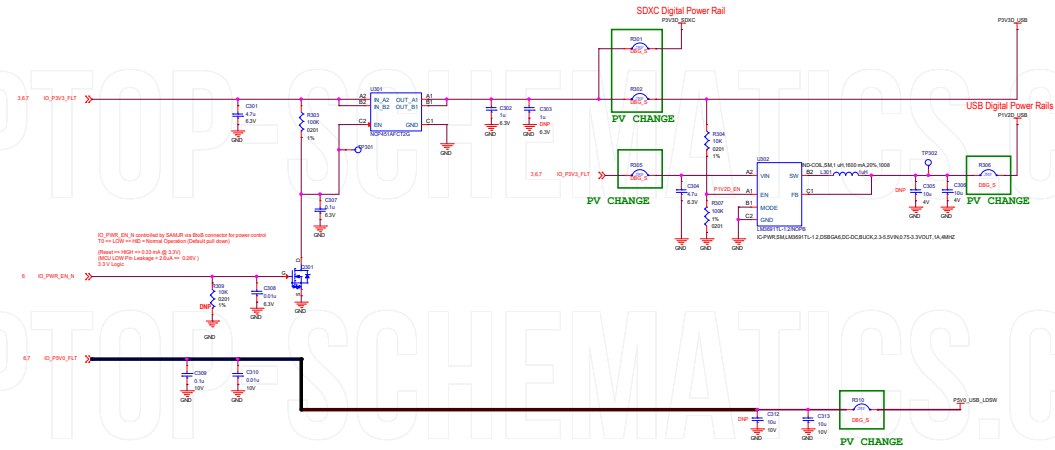
DNP = Not Installed Part.

DBG_D = EV/DV phase only

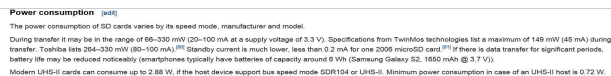
DBG_S = Short after design fixed

			Unit: mil					
Stack up 6L 0.7mm+/-0.075mm: 1-4-1+			impedance control	Single-end, 50Ω±10%	Single-end, 45Ω±10%	Differential, 100Ω±10%	Differential, 90Ω±10%	Differential, 85Ω±10%
Layer	material							
Top Surface		0.8						
L1	1/3 Oz copper+plating	1.2	L1(refer L2)	4.491	5.531	3.162/4.34	4.282/4.82	5.152/5.85
	EM285B 1080	2.71						
L2	1/3 Oz copper+plating	1.1						
	EM285B 1080	2.41						
L3	1/2OZ	0.6	L3(refer L2and L4)	3.271	4.051	3.002/7.84	3.682/6.92	3.952/5.55
	EM285 10mil core	10.0						
L4	1/2OZ	0.6	L4(refer L3 and L5)	3.271	4.051	3.002/7.84	3.682/6.92	3.952/5.55
	EM285B 1080	2.41						
L5	1/3 Oz copper+plating	1.1	L5(refer L4 and L6)					
	EM285B 1080	2.71						
L6	1/3 Oz copper+plating	1.2	L6(refer L5)	4.491	5.531	3.162/4.34	4.282/4.82	5.152/5.85
Bottom Surface		0.8						
Total		mil 27.64						
		um 0.70						

IO Power Tree

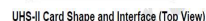


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MMC	Pin 1	Pin 2	Pin 3	Name	IO	Logic	Description
-	1	1	2	DAT3	IO	PP	SD Serial Data 3
-	2	3	3	CMD IO	PP	PP	Command, Response
-	4	4	5	VSS	S	S	Ground
-	4	4	4	VDD	S	S	Power
-	5	5	5	CLK	I	PP	Serial Clock
-	6	6	6	VSS	S	S	Ground
-	7	7	7	DAT0	IO	PP	SD Serial Data 0
-	8	8	8	DAT1	IO	PP	SD Serial Data 1 (memory cards)
-	8	8	8	WPST	O	OG	Interrupt Period (SDIO cards share pin via protocol)
-	9	9	1	DAT2	IO	PP	SD Serial Data 2
-	10	10	NC	-	-	-	Reserved
-	11	11	NC	-	-	-	Reserved

Pin #	Name	Type	Description
4	VDD1	Supply voltage	2.7V to 3.5V
7	RCLK+	Differential Signaling Input	Clock Input
8	RCLK-	Differential Signaling Input	Clock Input
10	VSS3	Ground	
11	D0+	Differential Signaling Input (FD) / Bidirectional (HD)	Input in default
12	D0-	Differential Signaling Input (FD) / Bidirectional (HD)	Input in default
14	VSS4	Ground	
14	VDD2	Supply voltage 2	1.70V to 1.95V
15	D1+	Differential Signaling Output (FD) / Bidirectional (HD)	Output in default
16	D1-	Differential Signaling Output (FD) / Bidirectional (HD)	Output in default
17	VSS8	Ground	



WITH OUT CARD		CARD INSERTED WRITE PROTECT : LOCK		CARD INSERTED WRITE PROTECT : UNLOCK	
W/P (#1) 	GND (#21) 	W/P (#1) 	GND (#21) 	W/P (#1) 	GND (#21)
C/D1 (#12) 	VSS (#11) 	C/D1 (#12) 	VSS (#11) 	C/D1 (#12) 	VSS (#11)

UHS-II Card Operation Modes

- SD Bus Interface Modes**
- DS - Default Speed up to 25MHz 3.3V signaling
 - HS - High Speed up to 50MHz 3.3V signaling
 - SDR12 - SDR up to 25MHz 1.8V signaling
 - SDR25 - SDR up to 50MHz 1.8V signaling
 - SDR50 - SDR up to 100MHz 1.8V signaling
 - SDR104 - SDR up to 208MHz 1.8V signaling (Optional)
 - DDR50 - DDR up to 50MHz 1.8V signaling (Optional for Standard Size Card)
- UHS-II Interface Modes**
- FD160 - Full Duplex mode up to 160MB/s at 52MHz in Range B
 - HD312 - Half Duplex with 2 Lanes mode up to 312MB/s at 52MHz in Range B (Optional)

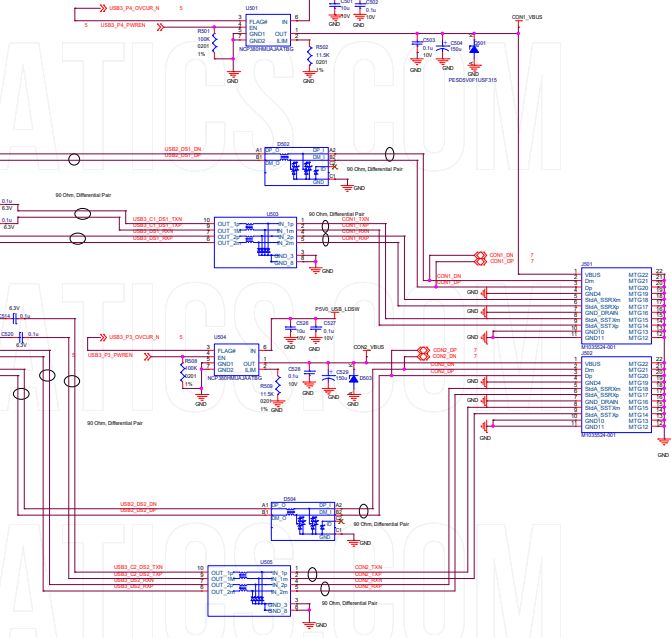
USB 3.0 Hub GL3523

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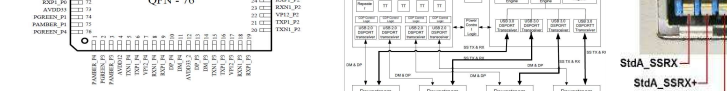
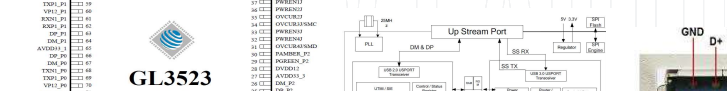
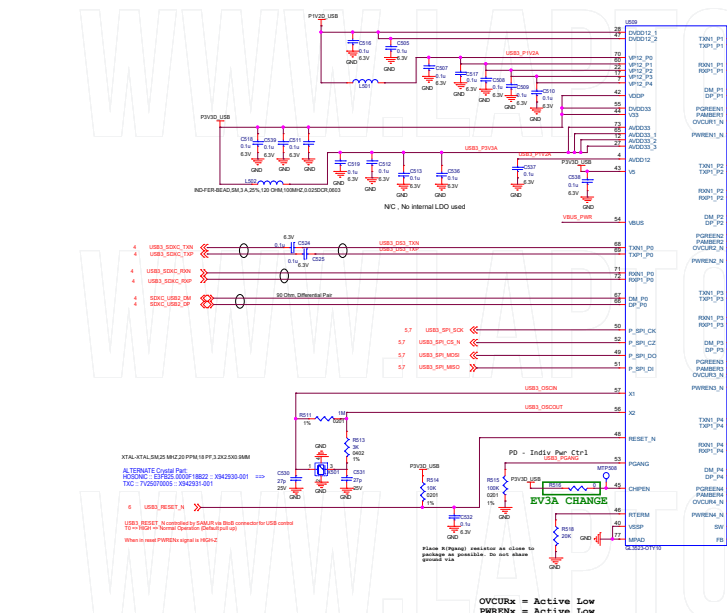
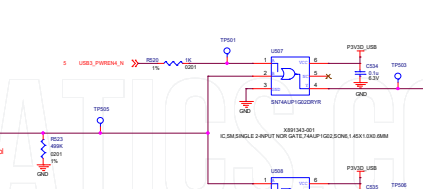
Q1: Note that the width of the signal traces is equal to the signal pitch between the two signals. This can be tolerated in a 100 ohm differential pair, as long as the signal traces are specified by 100 ohm differential pair, as specified by 100 ohm differential pair. The recommended board trace for intra-pair skew is no more than 5 mils (0.127 mm). Ideally, all signal pairs should be of equal length to ensure zero time difference. DisplayPort, however, allows for a maximum intra-pair skew. The time difference between signal pairs, of 2 Ds. The UI for high bit rate (1.7 Gbps/line), is 370 ps (nominal).

ZUI = 2*370ps = 740ps skew
PR4 (Inner Layer) => 180ps/in
PR4 (Outer Layer) => 150ps/in

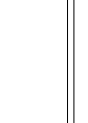
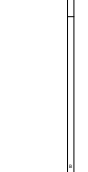
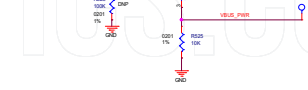
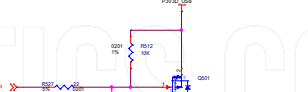
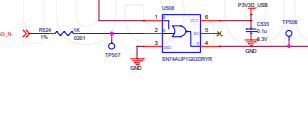
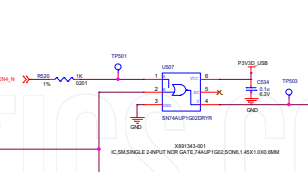
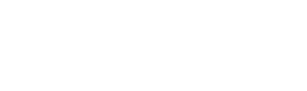
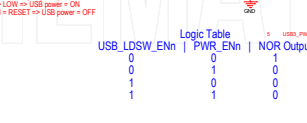
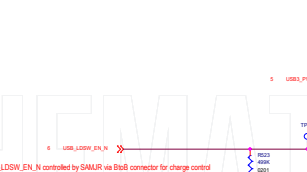
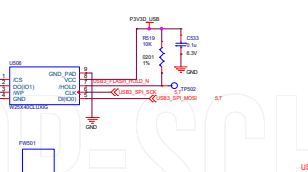
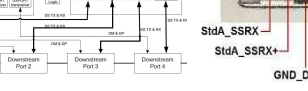
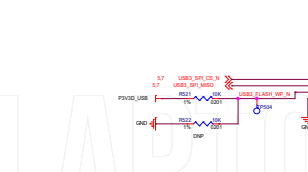
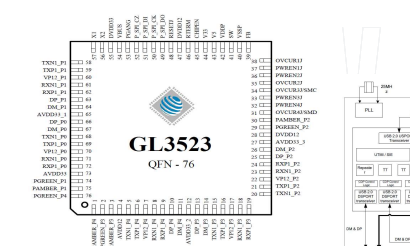
MC9380 Load Switch:
Active Discharge built in.
FETs: Active-low open-drain output, asserted during overcurrent, over-temperature, or reverse-voltage conditions.
SW: Active-LOW enable.
Place 0.1uF and 10uF caps close to switch.



USB_LDSW_EN_N controlled by SMUR via Rstb connector for charge control (External USB port power)
TO = LOW => USB power = ON
HIGH = RESET => USB power = OFF



USB 3.0 Connector Pinouts ^[1]			
Pin	Color	Signal name ("A" Connector)	Signal name ("B" Connector)
Shell	N/A	Shield	Metal housing
1	Red	VBUS	Power
2	White	D-	USB 2.0 differential pair
3	Green	D+	
4	Black	GND	Ground for power return
5	Blue	StdA_SSRX-	StdB_SSTX-
6	Yellow	StdA_SSRX+	StdB_SSTX+
7	N/A	GND_DRAIN	Ground for signal return
8	Purple	StdA_SSTX-	StdB_SSRX-
9	Orange	StdA_SSTX+	StdB_SSRX+



IO to SL Board to Board Connector

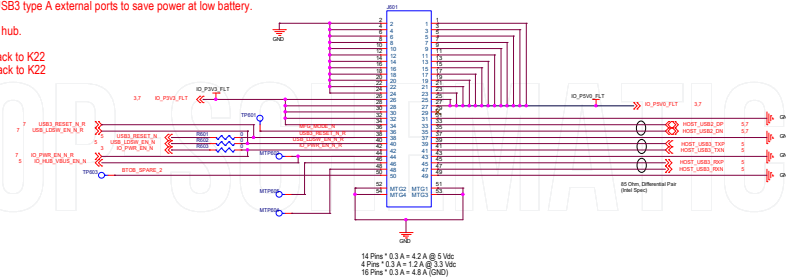
IO_PWR_EN_N = SAM JR signal to disable all IO board functionality (removes all power)

USB_LDSW_EN_N = Power down both USB3 type A external ports to save power at low battery.



USB3_RESET_N = Reset USB 3.0 4 port hub.



HID_USB2_DP = USB signal from Hub back to K22


HID_USB2_DN = USB signal from Hub back to K22



Pin	Signal	Function	IO
MT9702	IO_PWR_EN_N_R		6
MT9705	USB3_RESET_N_R		
TP308	USB3_GPI_MISO		5
TP711	USB3_GPI_MOSI		5
TP713	USB3_GPI_SCK		5
TP715	USB3_GPI_CS_N		5
MT9720	USB_LDOEN_EN_N_R		6



5.6 HOST_USBD_0N   NETFW33



5.6 HOST_USBD_0N   NETFW36


QED  NETFW31

Please wait to **SEND** the board to board manager

Please wait to **SEND** the board to board manager



5.6 CONN_0N   NETFW16



5.6 CONN_0N   NETFW19


QED  NETFW21

Please wait to **SEND** USB connectors

Please wait to **SEND** USB connectors

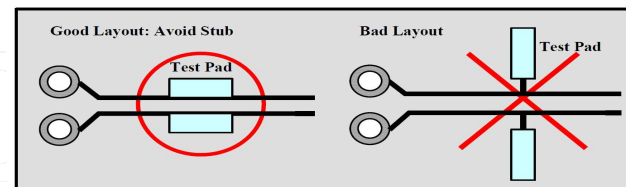
5.6 CONN_DP   NETFW28

5.6 CONN_DP   NETFW30

QED  NETFW33

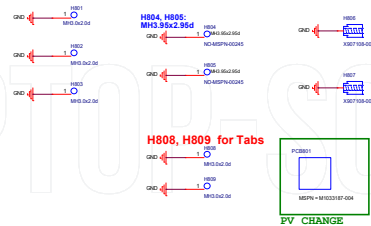
Please wait to **SEND** USB connectors

Please wait to **SEND** USB connectors



Mechanical Holes and Shielding

Holes updated: 4x 2.0mm PTH, 2x 2.95mm PTH, 2x 2.5mm PEM



Shield Removed for EV1
-EV1 will use FOAM